هيئة تقويم التعليم والتدريب
Education & Training Evaluation Commission

2023
TP-153

Course Specification
(Bachelor)

Course Title:	**VLSI Design**
Course Code:	**CEN 1416**
Program:	**Bachelor in Computer Engineering**
Department:	**Computer Engineering**
College:	**Faculty of Computers and Information Technology**
Institution:	**University of Tabuk**
Version:	**1.0**
Last Revision Date:	**27 July 2022**

Table of Contents

A. General information about the course:

1. Course Identification

1. Credit hours: (3)					
2. Course type					
A.	☐University	☐College	☒ Department	☐Track	☐Others
B.	☐Required		☒ Elective		
3. Level/year at which this course is offered: (9th Level/5th year)					
4. Course general Description:					
Large-scale MOS design: MOS transistors, static and dynamic MOS gates, stick diagrams, programmable logic array design, MOS circuit fabrication, design rules, resistance and capacitance extraction, power and delay estimates, scaling, MOS combinational and sequential logic design, register and clocking schemes, memory, data-path, and control unit design. Elements of computer-aided circuit analysis and layout techniques.					
5. Pre-requirements for this course (if any)**:**					
• Electronic Devices CEN 1304 • Computer Architecture CEN 1403					
6. Co-requisites for this course (if any)**:**					
None					
7. Course Main Objective(s):					
1. Knowledge on fundamentals of MOS transistors and CMOS logic. **2. Understand programmable logic array design.** **3. Ability to analyze and synthesize MOS circuits.** **4. Analyze MOS combinational and sequential logic circuits.** **5. Design MOS logic circuits.**					

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	45	100%
2	E-learning	0	
3	Hybrid • Traditional classroom	0	

No	Mode of Instruction	Contact Hours	Percentage
	• E-learning		
4	Distance learning	0	

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	**Lectures**	45
2.	**Laboratory/Studio**	0
3.	**Field**	0
4.	**Tutorial**	0
5.	**Others (specify)**	0
Total		45

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of PLOs aligned with program	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
1.1	Knowledge on fundamentals of MOS transistors and CMOS logic.	**K4**	• Lectures • Discussion in groups Problem solving.	Class work Midterms Final Exam
1.2	Define programmable logic array design.	**K5**	• Lectures • Discussion in groups Problem solving.	Class work Midterms Final Exam
2.0	**Skills**			
2.1	Explain the techniques and develop the documents related to digital image processing.	**S2**	Lectures Discussion in groups Problem solving.	Class work Midterms Final Exam
2.2	Ability to analyze and synthesize MOS circuits.	**S3**	Lectures Discussion in groups Problem solving.	Class work Midterms Final Exam
…	Analyze MOS combinational and sequential logic circuits.	**S4**	Lectures Discussion in groups	Class work Midterms Final Exam

Code	Course Learning Outcomes	Code of PLOs aligned with program	Teaching Strategies	Assessment Methods
			Problem solving.	
3.0	**Values, autonomy, and responsibility**			
3.1	Evaluate the knowledge, tools and techniques covered in the course to digital image processing	**V1**	Lectures Discussion in groups Problem solving.	Class work Midterms Final Exam
3.2	Design MOS logic circuits.	**V2**	Lectures Discussion in groups Problem solving.	Class work Midterms Final Exam

C. Course Content

No	List of Topics	Contact Hours
1.	**MOS transistors.**	3
2.	**Static and Dynamic MOS gates, stick diagrams**	3
3.	**Programmable logic array design – part 1**	3
4.	**Programmable logic array design – part 2**	3
5..	**MOS circuit fabrication and design rules**	3
6.	**Resistance and Capacitance extraction**	3
7.	**Power and Delay estimates, scaling**	3
8.	**Combinational and Sequential logic design – part 1**	3
9.	**Combinational and Sequential logic design – part 2**	3
10.	**Register and clocking schemes – part 1**	3
11.	**Register and clocking schemes – part 2**	3
12.	**Memory and data-path**	3
13.	**Control unit design**	3
14.	**Elements of computer-aided circuit analysis**	3
15.	**Elements of layout techniques**	3
Total		**45**

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	**Classwork**	**1-15**	**20%**
2.	**Midterms**	**6-11**	**40%**
3.	**Final exam.**	**17**	**40%**

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources

Essential References	• Thomas Dillinger, VLSI Design Methodology Development, Pearson India; 1st edition (July 18, 2019), ISBN: 978-0135732410 • Weste et al., CMOS VLSI Design 4e: A circuits and systems perspective, PEARSON INDIA; 4th edition (January 1, 2010), ISBN: 978-9332542884
Supportive References	**Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu,** *VLSI Physical Design: From Graph Partitioning to Timing Closure,* Springer; 2nd ed. 2022 edition (June 16, 2022), ISBN: 978-3030964146
Electronic Materials	**None**
Other Learning Materials	**None**

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	Classrooms
Technology equipment (projector, smart board, software)	Smart Board - Data-Show – Whiteboard - Wifi Connection
Other equipment (depending on the nature of the specialty)	**None**

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of Teaching	Faculty, Program Leaders, and Advisory Board	Both Direct and Indirect
	Students	Indirect
Effectiveness of Students Assessment	Faculty, Program Leaders, Advisory Board, and Independent Opinion	Both Direct and Indirect
Quality of Learning Resources	Faculty, Students, and Advisory Board	Indirect
The Extent to which CLOs have been Achieved	Faculty, Program Leaders, Advisory Board, and Independent Opinion	Direct (as in section B) and Indirect/Surveys
	Students	Indirect
Other	-	-

Assessors (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)

Assessment Methods (Direct, Indirect)

G. Specification Approval

COUNCIL /COMMITTEE	

REFERENCE NO.	
DATE	