هيئة تقويم التعليم والتدريب
Education & Training Evaluation Commission

2023
TP-153

Course Specification
(Bachelor)

Course Title:	**Programmable Logic Devices**
Course Code:	**CEN1407**
Program:	**Bachelor in Computer Engineering**
Department:	**Computer Engineering**
College:	**Faculty of Computers and Information Technology**
Institution:	**University of Tabuk**
Version:	**1.0**
Last Revision Date:	**27 July 2022**

Table of Contents

A. General information about the course:

1. Course Identification

1. Credit hours: (4)					
2. Course type					
A.	☐University	☐College	☒ Department	☐Track	☐Others
B.	☒ Required		☐Elective		
3. Level/year at which this course is offered: (8/4)					
4. Course general Description:					
5. Pre-requirements for this course (if any)**:**					
Digital Logic (2) CEN 1302					
6. Co-requisites for this course (if any)**:**					
7. Course Main Objective(s):					

1. Understand the basics of digital design using different types of programmable logic devices such as PAL, PLA, PROM, CPLDs, and FPGA as well as an understanding of the underlying technologies and architectures of these devices.
2. Develop and understand the available prefabricated IP blocks on modern CPLDs and FPGAs and learn how to use them in their designs.
3. Apply VHDL programming language in the design of PLDs, CPLDs, and FPGA.
4. Simulate & synthesize VHDL structures.
5. Apply advanced methods for testing and designing advanced digital systems using VHDL.
6. Identify and implement coding best practices.

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	75	100%
2	E-learning		
3	Hybrid ● Traditional classroom ● E-learning		
4	Distance learning		

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	Lectures	45
2.	Laboratory/Studio	30
3.	Field	
4.	Tutorial	
5.	Others (specify)	
Total		75

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of PLOs aligned with program	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
1.1	Define and state the basics of PLDs, CPLDs, FPGA	K1,K2	Lectures, Lab sessions	Class Works, Quizzes, Assignments, Exams, Labwork.
1.2	Describe the architecture of different PLDs, CPLDs and FPGAs technologies.	K1,K4	Lectures, Lab sessions	Class Works, Quizzes, Assignments, Exams, Labwork.

Code	Course Learning Outcomes	Code of PLOs aligned with program	Teaching Strategies	Assessment Methods
1.3	Define and describe the VHDL structures and state how it fits into the FPGA design flow.	K1,K5	Lectures, Lab sessions	Class Works, Quizzes, Assignments, Exams, Labwork.
1.4	Outline advanced methods for designing and testing advanced digital systems using VHDL.	K3	Lectures, Lab sessions	Class Works, Quizzes, Assignments, Exams, Labwork.
1.5	State and simulate a basic VHDL design	K2,K3	Lectures, Lab sessions	Exams, Labwork.
1.6	Define and implement coding best practices	K2,K4	Lectures, Lab sessions	Exams, Labwork.
2.0	**Skills**			
2.1	Compare between PLD, CPLDs and FPGAs	S1, S4	Lectures, Lab sessions	Class Works, Quizzes, Assignments, Exams, Labwork..
2.2	Differentiate between the underlying technologies and architectures of CPLDS and FPGAs	S1,S3	Lectures, Lab sessions	Class Works, Quizzes, Assignments, Exams, Labwork.
2.3	Develop a basic VHDL design	S2, S3, S4	Lectures, Lab sessions	Exams, Labwork.
3.0	**Values, autonomy, and responsibility**			
3.1	To demonstrate the effectiveness of team work	V2	Lectures, Lab sessions	Exams, Labwork.

C. Course Content

No	List of Topics	Contact Hours
1.	▪ Combinational and Sequential circuits Review ▪ Lab: Design of combinational circuits using Altera MaxPLUS2	5
2.	▪ Introduction to programmable logic Devices (PLDs) ▪ Lab: Design of advanced combinational and Sequential circuits using Altera MaxPLUS2	5
3.	▪ Programmable Logic Arrays (PLA) design and Implementation ▪ Lab: Implementation of basic PLAs using Altera MaxPLUS2	5
4.	▪ Programmable Arrays Logic (PAL) and Generic Array Logic (GAL) design and Implementation ▪ Lab: Design of PALs using Altera MaxPLUS2	5
5.	▪ design Programmable Read Only Memory and Implementation ▪ Lab: of PROMs using decoder	5
6.	▪ Introduction to Complex PLDs (CPLDs) ▪ Lab Design of CPLDs using CPLD/FPGA kit (basics)	5
7.	▪ CPLDs design and Implementation ▪ Lab: Design of CPLDs using CPLD/FPGA kit	5
8.	▪ Introduction to Field Programmable Gate Array (FPGA) ▪ Lab: Design of CPLDs using CPLD/FPGA kit (basics)	5
9.	▪ FPGA Design and Implementation ▪ Lab: Design of CPLDs using CPLD/FPGA kit (basics)	5

10.	▪ CPLDs, FPGA applications ▪ Lab: Design of advanced digital circuits using CPLD/FPGA kit	5
11.	▪ Introduction to VHDL programming Language ▪ Lab: Writing VHDL codes for realizing the logic gates	5
12.	▪ Entity and Architecture. Behavioral, data flow and structural specifications ▪ Lab: Writing VHDL codes including entity and the three types of architecture	5
13.	▪ VHDL: basic concepts, basic language constructs, simulation and VHDL synthesis and implementation of VHDL ▪ Lab: Design of simple combinational circuits using VHDL programming language and CPLD FPGA Lab trainer	5
14.	▪ Design of Combinational Circuits using VHDL ▪ Lab: Design of advanced combinational circuits using VHDL programming language and CPLD FPGA Lab trainer	5
15.	▪ Designing Arithmetic circuits in VHDL and VHDL for multi-component digital system ▪ Lab: Design of Arithmetic circuits using VHDL programming language and CPLD FPGA Lab trainer	5
Total		**75**

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	Assignments, Quizzes, Labwork	1-15	30%
2.	First Midterm Exam	6 - 8	15%
3.	Second Midterm Exam	11-12	15%
4.	Final Semester Exam	14-17	40%

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources

Essential References	1. Fundamentals of Digital Logic with VHDL Design with CD-ROM, 4/E, Mc-Graw Hill Higher Education, Stephen Brown, 2022, ISBN-10: 0073380725, ISBN-13: 978-0073380728. 2. The Design Warrior's Guide to FPGAs, Devices, Tools and Flows, Clive "Max" Maxfield, 1/E, Newnes, 2004, ISBN-10: 0750676043, ISBN-13: 978-0750676045. 3. VHDL for Programmable Logic, Kevin Skahill, Pearson Education, 2/E, 2008. 4. Jr. Charles H. Roth, Lizy K. John, Digital Systems Design Using VHDL, 3/E, Cengage Learning, 2017, ISBN-10: 1305635140, ISBN-13: 978-1305635142.
Supportive References	

Electronic Materials	Faculty member's web sites, SDL, University Library
Other Learning Materials	ISE software environment

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	Classroom, laboratory
Technology equipment (projector, smart board, software)	White board, Data show projector
Other equipment (depending on the nature of the specialty)	TBA

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of Teaching	Faculty, Program Leaders, and Advisory Board	Both Direct and Indirect
	Students	Indirect
Effectiveness of Students Assessment	Faculty, Program Leaders, Advisory Board, and Independent Opinion	Both Direct and Indirect
Quality of Learning Resources	Faculty, Students, and Advisory Board	Indirect
The Extent to which CLOs have been Achieved	Faculty, Program Leaders, Advisory Board, and Independent Opinion	Direct (as in section B) and Indirect/Surveys
	Students	Indirect
Other	-	-

Assessors (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)

Assessment Methods (Direct, Indirect)

G. Specification Approval

COUNCIL /COMMITTEE	
REFERENCE NO.	
DATE	