Course Specification

(Bachelor)

Course Title: Digital Logic (2)	
Course Code: CEN 1302	
Program: Bachelor in Computer Engineering	
Department: Computer Engineering	
College: Faculty of Computers and Information Technology	
Institution: University of Tabuk	
Version: 1.0	
Last Revision Date: 27 July 2022	

Table of Contents

A. General information about the course:

1. Course Identification

1. Credit hours: (4)

2. Course type

A.	☐University	☐College	☒ Department	☐Track	☐Others
B.	☒ Required		☐Elective		

3. Level/year at which this course is offered: 5ᵗʰ Level / 3th Year

4. Course general Description:

This course covers the Basic knowledge on synchronous sequential machines, Memory elements, Sequential circuit analysis, Sequential circuits design, Programmable Logic Devices, Registers and Register Transfers and Memory Basics.

5. Pre-requirements for this course (if any):

CEN 1201

6. Co-requisites for this course (if any):

N/A

7. Course Main Objective(s):

The main purpose for this course is :
- Understand fundamentals of synchronous sequential machines.
- Understand memory elements.
- Understand programmable logic devices.
- Ability to analyze and synthesize sequential circuits.
- Analyze digital systems, registers, counters, and sequencing.
- Design efficient sequential circuits.

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	75	100%
2	E-learning		
3	Hybrid ● Traditional classroom ● E-learning		
4	Distance learning		

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	**Lectures**	45
2.	**Laboratory/Studio**	30
3.	**Field**	
4.	**Tutorial**	
5.	**Others (specify)**	
Total		

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of PLOs aligned with program	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
1.1	Describe fundamental of synchronous sequential systems.	K1	● Lectures	Exams , Labwork , Quizzes, Assignments
1.2	State the memory elements and programmable logic devices.	K3, K4, K5	● Lectures	Exams , Labwork , Quizzes, Assignments
2.0	**Skills**			
2.1	Analyze and synthesize sequential logic circuits.	S1, S4	● Discussion ● Lab Sessions	Exams
2.2	Analyze digital systems involving registers, counters, and sequencing.	S4	● Group discussions ● Case studies ● Lab Sessions	Exams , Labwork , Quizzes, Assignments
2.3	Design efficient sequential circuits.	S2, S3	● Lectures ● Discussions ● Lab Sessions	Exams , Labwork , Quizzes, Assignments
3.0	**Values, autonomy, and responsibility**			

Code	Course Learning Outcomes	Code of PLOs aligned with program	Teaching Strategies	Assessment Methods
3.1	Demonstrate the effectiveness of teamwork.	V2	● Case studies ● Lab Sessions	Exams , Labwork , Quizzes, Assignments

C. Course Content

No	List of Topics	Contact Hours
1.	**Sequential logic circuits.**	5
2.	**Sequential logic circuits analysis.** **Lab:** **Sequential Circuits**: Up-Down Counter with Enable, Design using State Diagram	5
3.	**Sequential logic circuits simulation.** **Lab:** **Sequential Circuits**: Counter with specified sequence	5
4.	**Sequential logic circuits design (Part 1).** **Lab:** **Sequential Circuits**: Latches and Flip-flops, Registers and Counters	5
5.	**Sequential logic circuits design (Part 2).** **Lab:** Sequential Circuits Design	5
6.	**Registers** **Lab:** State and Registers	5
7.	**Register transfers** **Lab : Register transfers and micro-operations**: Register Transfer Language, Register Transfer, Bus and Memory Transfers	5
8.	**Register Micro-operations** **Lab:** Register transfers and micro-operations: Arithmetic Microoperations, Logic Microoperations, Shift Microoperations, Arithmetic Logic Shift Unit	5
9.	**Counters (Part 1): Synchronous** **Lab:** Sequential Circuits: Synchronous counters	5
10.	**Counters (Part 2): Asynchronous** **Lab:** Sequential Circuits: Asynchronous counter	5
11.	**Ripple Counters** **Lab:** Sequential Circuits: Ripple counter	5
12.	**Synchronous Binary Counters.** **Lab:** Sequential Circuits: Synchronous Binary counter	5

13.	**Memory** <u>**Lab Work:**</u> Memory	5
14.	**Read and Write operations** <u>**Lab:**</u> Read and Write operations	5
15.	**Properties of Memory**	5
	Total	**75**

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	Quizzes, Assignments	2-15	20%
2.	Lab work	14 or 15	10%
3.	Mid-Exam 1	6 or 7	15%
4.	Mid-Exam 2	11 or 12	15%
5.	Final Exam	After 16	40%

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources

Essential References	**Advanced Digital Design with the Verilog HDL / by Michael D. Ciletti / 978-0136019282 / Prentice Hall / 2 edition / 2010 / Digital Design with HDL**
Supportive References	
Electronic Materials	www.wowebook.com Faculty members sites
Other Learning Materials	**Blackboard Platform**

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	**Classroom , Digital Logic Lab, KL3300xx**
Technology equipment (projector, smart board, software)	**projector**
Other equipment (depending on the nature of the specialty)	**MATLAB and SIMULINK**

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of Teaching	Faculty, Program Leaders, and Advisory Board	Both Direct and Indirect
	Students	Indirect
Effectiveness of Students Assessment	Faculty, Program Leaders, Advisory Board, and Independent Opinion	Both Direct and Indirect
Quality of Learning Resources	Faculty, Students, and Advisory Board	Indirect
The Extent to which CLOs have been Achieved	Faculty, Program Leaders, Advisory Board, and Independent Opinion	Direct (as in section B) and Indirect/Surveys
	Students	Indirect
Other	-	-

Assessors (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)

Assessment Methods (Direct, Indirect)

G. Specification Approval

COUNCIL /COMMITTEE	
REFERENCE NO.	
DATE	