هيئة تقويم التعليم والتدريب
Education & Training Evaluation Commission

2023
TP-153

Course Specification
(Bachelor)

Course Title:	**Computer Architecture**
Course Code:	**CEN 1252**
Program:	**Bachelor in Computer Science**
Department:	**Computer Engineering**
College:	**Computers and Information Technology**
Institution:	**University of Tabuk**
Version:	**1.0**
Last Revision Date:	**27 July 2022**

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A. General information about the course:

1. Course Identification

1. Credit hours: (3)					
2. Course type					
A.	☐ University	☐ College	☒ Department	☐ Track	☐ Others
B.	☒ Required		☐ Elective		
3. Level/year at which this course is offered: (Level 4/Year 2)					
4. Course general Description:					
This course provides an in-depth exploration of advanced concepts in computer architecture, offering a comprehensive understanding of the structure, functionality, and performance aspects of modern computer systems. From the fundamental components to advanced techniques, students will delve into the intricacies of processor design, memory systems, and parallel processing.					
5. Pre-requirements for this course (if any):					
Computer Organization and Assembly Language -CSC1202					
6. Co-requisites for this course (if any):					
N/A					
7. Course Main Objective(s):					
● Describe the organization of RAM. ● Distinguish among different caching techniques. ● Describe the principal issues related to cache memory organization and performance. ● Distinguish between virtual memory schemes based upon segmentation and based upon paging. ● Describe the differences between asynchronous and synchronous buses, as well as the importance of bus arbitration schemes to the effective operation of the bus. ● Distinguish between Micro-programmed and Hardwired processor control, and describe the benefits of each approach. ● Analyze the nature of a computer instruction set, explore the interaction between the CPU -memory and I/O peripheral devices.					

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	45	100%
2	E-learning		
3	Hybrid ● Traditional classroom ● E-learning		
4	Distance learning		

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	**Lectures**	45
2.	**Laboratory/Studio**	0
3.	**Field**	0
4.	**Tutorial**	0
5.	**Others (specify)**	0
Total		45

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of PLOs aligned with program	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
1.1	Recognize the general organization and architecture of computers	K2	● **Lecture** ● **Group discussion**	● **Exams** ● **Individual reports** ● **Class work**
1.2	Describe computers major components and study their functions	K2	● **Research activities** ● **Case studies**	• **Exams** • **Presentations** **Class work**
2.0	**Skills**			
2.1	Explain the techniques and develop the	S3,S4	● **Lecture** ● **Group work**	● **Exams** ● **Reports**

Code	Course Learning Outcomes	Code of PLOs aligned with program	Teaching Strategies	Assessment Methods
	documents related to computer architecture.		• Research activities • Case studies	
2.2	Compare the knowledge, tools and techniques covered in computer architecture.	S3	• Lecture • Group discussion • Research activities • Case studies	• Exams • Reports • Class Work
3.0	**Values, autonomy, and responsibility**			
	N/A			

C. Course Content

No	List of Topics	Contact Hours
1.	**An Overview of Computer Systems:** **Introduction to computer architecture, Historical perspective and evolution of computer systems, Basic components and their interconnections.**	**3**
2.	**Performance Issues in Computer Systems (Part1):** **Designing for performance: Microprocessor speed, Performance balance, Improvements in chip organization and architecture. Multicore, MICs, GPGPUs, Amdahl's Law, Little's Law**	**3**
3.	**Performance Issues in Computer Systems (Part2):** **Basic measures of computer performance: Clock speed, Instruction execution rate. Calculating the mean: Arithmetic mean, Harmonic mean, Geometric mean. Benchmark principles**	**3**
4.	**Advanced Cache Memory Techniques (Part1):** **Cache organization and mapping techniques, Cache coherence and consistency, Multi-level caching.**	**3**
5.	**Advanced Cache Memory Techniques (Part2):** **Cache replacement policies, Virtual memory and its interaction with caching, Emerging trends in cache design.**	**3**
6.	**Input/Output Modules:** **External devices, I/O modules, Programmed I/O, Direct memory access, Interrupt-driven I/O, Direct Cache Access, I/O channels and processors**	**3**
7.	**Processor Structure and Function:** **Processor organization, Register organization, Instruction cycle, The x86 processor family, Instruction pipelining, The Arm processor.**	**3**
8.	**Reduced Instruction Set Computers (RISC):**	**3**

	Instruction execution characteristics, The use of a large register file, Reduced instruction set architecture, Reduced instruction set architecture, RISC pipelining, Compiler-based register optimization, RISC versus CISC controversy.	
9.	Instruction-Level Parallelism and Superscalar Processors: Superscalar versus Superpipelined, Design issues: Instruction-level parallelism, Machine parallelism, Instruction issue policy, Register renaming, Branch prediction, Superscalar execution, Superscalar implementation.	3
10.	Parallel Processing (Part1): Multiple processor organizations: Types of parallel processor systems, Parallel organizations. Symmetric multiprocessors: Organization, Multiprocessor operating system design considerations. Cache coherence and the MESI protocol: Software solutions, Hardware solutions, The MESI protocol	3
11.	Parallel Processing (Part2): Multithreading and chip multiprocessors: Implicit and explicit multithreading, Approaches to explicit multithreading. Clusters, Nonuniform memory access: Motivation, Organization, NUMA Pros and cons. Cloud computing.	3
12.	Control Unit Operation (Part1): Micro-operations: The fetch cycle, The indirect cycle, The interrupt cycle, The execute cycle, The instruction cycle.	3
13.	Control Unit Operation (Part2): Control of the processor, Functional requirements, Control signals, Internal processor organization, The Intel 8085. Hardwired implementation: Control unit inputs, Control unit logic.	3
14.	Microprogrammed Control (Part1): Basic concepts: Microinstructions, Microprogrammed control unit, Wilkes control, Advantages and disadvantages. TI 8800: Microinstruction format, Microsequencer, Registered ALU	3
15.	Microprogrammed Control (Part2): Microinstruction sequencing: Design considerations, Sequencing techniques, Address generation, LSI-11 microinstruction sequencing. Microinstruction execution: Taxonomy of microinstructions, Microinstruction encoding, LSI-11 Microinstruction execution, IBM 3033 Microinstruction execution	3
Total		45

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1	Class Works *(Quizzes, Group Discussion, Reports)* and Home works *(Individual Assignments, Group Assignments)*	1 - 15	30%
2	Mid-Term 1	6-7	15%
3	Mid-Term 2	11-13	15%
4	Final Exam	17	40%

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources

Essential References	Computer Organization and Architecture (11th Edition) , Pearson, 2018, by William Stallings, ISBN-10 : 0134997190, ISBN-13 : 978-0134997193
Supportive References	1) The Architecture of Computer Hardware and Systems Software, Irv Englander, 4th Edition, 2009, Willey. 2) Systems Architecture, Stephen Burd, 2010, 6th Edition, Cengage Learning.
Electronic Materials	Saudi Digital Library (SDL) (www.sdl.edu.sa)
Other Learning Materials	Linda Null & Julia Lobur, The Essentials of Computer Organization and Architecture, 2nd edition, ISBN: 0-76373769-0

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	Classroom (35 seats)
Technology equipment (projector, smart board, software)	White board, Data show projector
Other equipment (depending on the nature of the specialty)	

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of Teaching	Faculty, Program Leaders, and Advisory Board	Both Direct and Indirect
	Students	Indirect

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of Students Assessment	Faculty, Program Leaders, Advisory Board, and Independent Opinion	Both Direct and Indirect
Quality of Learning Resources	Faculty, Students, and Advisory Board	Indirect
The Extent to which CLOs have been Achieved	Faculty, Program Leaders, Advisory Board, and Independent Opinion	Direct (as in section B) and Indirect/Surveys
	Students	Indirect
Other	-	-

Assessors (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)

Assessment Methods (Direct, Indirect)

G. Specification Approval

COUNCIL /COMMITTEE	
REFERENCE NO.	
DATE	