



Course Specification

— (Bachelor)

Course Title: Digital Logic (1)

Course Code: CEN 1201

Program: Bachelor in Computer Engineering

Department: Computer Engineering

College: Faculty of Computers and Information Technology

Institution: University of Tabuk

Version: 1.0

Last Revision Date: 27 July 2022



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A. General information about the course:

1. Course Identification

1. Credit hours: (4)

2. Course type

A. University College Department Track Others
B. Required Elective

3. Level/year at which this course is offered: 4th Level / 2nd Year

4. Course general Description:

Digital Logic (1) course covers the Digital systems and Binary Numbers including Binary Numbers, Number Base Conversions, Octal and Hexadecimal Numbers, Complements, Signed Binary Numbers, Binary Codes, Binary Storage and Registers, Binary Logic. Also, it covers Boolean Algebra and Logic Gates, Gate-Level Minimization, Combinational Logic, Synchronous Sequential Logic and Registers and Counters.

5. Pre-requirements for this course (if any):

MATH 1251

6. Co-requisites for this course (if any):

N/A

7. Course Main Objective(s):

The main purpose for this course is:

- Knowledge of fundamental Boolean principles and their application to digital design.
- Understand combinational and sequential digital/logic circuits, and modular design techniques. Ability to analyze and synthesize logic circuits.
- Analyze digital systems involving logic gates; multiplexers, demultiplexers, decoders, encoders, flip-flops, and counters.
- Design efficient combinational arithmetic and data processing circuits.
- Design efficient sequential arithmetic and data processing circuits.

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	75	100%
2	E-learning		
3	Hybrid		



No	Mode of Instruction	Contact Hours	Percentage
	<ul style="list-style-type: none"> ● Traditional classroom ● E-learning 		
4	Distance learning		

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	Lectures	45
2.	Laboratory/Studio	30
3.	Field	
4.	Tutorial	
5.	Others (specify)	
Total		

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of PLOs aligned with program	Teaching Strategies	Assessment Methods
1.0	Knowledge and understanding			
1.1	Recognize the concepts of mathematics, science and engineering.	K1	<ul style="list-style-type: none"> ● Lectures ● Group Discussions 	Lab work, Assignments, Quizzes, Exams
1.2	Demonstrate fundamental of Boolean principles and their application to digital design.	K3, K4	<ul style="list-style-type: none"> ● Lectures 	Exams, Lab work, Assignments
1.3	Demonstrate combinational and sequential digital/logic circuits, and modular design techniques.	K5	<ul style="list-style-type: none"> ● Lectures ● Group Discussions 	Exams
2.0	Skills			
2.1	Analyze and synthesize logic circuits.	S2	<ul style="list-style-type: none"> ● Lectures ● Lab Sessions 	Lab work, Assignments, Exams
2.2	Analyze digital systems involving logic gates; multiplexers, demultiplexers, decoders, encoders, flip-flops, and counters.	S1		



Code	Course Learning Outcomes	Code of PLOs aligned with program	Teaching Strategies	Assessment Methods
2.3	Develop efficient combinational and sequential arithmetic and data processing circuits.	S2		
3.0	Values, autonomy, and responsibility			
3.1	Demonstrate the effectiveness of teamwork.	V2	<ul style="list-style-type: none"> ● Lectures, textbooks, provided handouts, references. ● Lab Sessions 	Lab work, Assignments, Quizzes, Exams

C. Course Content

No	List of Topics	Contact Hours
1.	Binary Systems: Number Base Conversions. Lab: Digital Logic Gates: Basic Logic, Alternate Construction of Basic Gates	5
2.	Binary Systems: Complements, Binary Codes, Binary Storage and Operations. Lab: Digital Logic Gates: Simple Digital Circuit, DeMorgan's Theorems, Dual of a function	5
3.	Boolean Algebra and Logic Gates, Basic Theorems and Boolean Functions. Lab: Boolean Algebra and Functions: Postulates and Theorem of Boolean Algebra, Logic diagram and Boolean expression	5
4.	Canonical and Standard Forms, Other Logic Operations. Lab: Boolean Algebra and Functions: Logic diagram from sum of minterms, Short Theory Question	5
5.	Digital Logic Gate, Gate-Level Minimization. Lab: Gate-Level Minimization: implementation of different logic functions with 2 variables, 3 variables and 4 variables.	5
6.	The Map Method, Two, Three and Four-Variable Map. Lab: Simplification of Boolean functions using Karnaugh Maps: Two-Variable Karnaugh Map, Three-Variable Karnaugh Map, Four-Variable Karnaugh Map	5
7.	Combinational Logic, Combinational Circuits, Analysis Procedure. Lab: Combinational Circuits: Analysis of Combinational Circuit, Design from Truth Table	5



8.	Analysis Procedure and Design Procedure. Lab: Design of Combinational Circuit from Truth Table	5
9.	Binary Adder-Subtractor, Decimal Adder, Binary Multiplier. Lab: Adders and Subtractors: Half Adder, Full Add, Comparator	5
10.	Magnitude Comparator, Decoders, Encoders, and Multiplexers. Lab: Combinational Logic Modules – Decoders and Multiplexers	5
11.	Synchronous sequential logic. Lab: Design of Synchronous Sequential Circuits: Sequential Circuit Design Steps, Sequence Recognizer, Deriving the State Diagram, Deriving the State Table, State Assignment, General Structure of Sequence Recognizer, Deriving the Excitation Table, Circuit Diagram of the Sequence Recognizer	5
12.	Synchronous sequential logic: analysis and design procedure. Lab: Design a sequential circuit using flip-flops	5
13.	Registers and Counters. Lab: Latches, Flip Flops and Counters	5
14.	Registers: Analysis and Design procedure. Lab: Design of Registers	5
15.	Counters: Analysis and Design procedure. Lab: Design of Counters	5
Total		75

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	Assignments, Quizzes	2-15	20%
2.	Lab work	14 or 15	10%
3.	Mid-Exam 1	6 or 7	15%
4.	Mid-Exam 2	11 or 12	15%
5.	Final Exam	After 16	40%

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources



Essential References	<ul style="list-style-type: none"> Advanced Digital Design with the Verilog HDL / by Michael D. Ciletti / 978-0136019282 / Prentice Hall / 2 edition / 2010 / Digital Design with HDL
Supportive References	
Electronic Materials	www.wowebook.com Faculty members sites
Other Learning Materials	Blackboard Platform

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	Classroom
Technology equipment (projector, smart board, software)	projector
Other equipment (depending on the nature of the specialty)	Digital Logic Lab, KL3300xx, MATLAB and SIMULINK

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of Teaching	Faculty, Program Leaders, and Advisory Board	Both Direct and Indirect
	Students	Indirect
Effectiveness of Students Assessment	Faculty, Program Leaders, Advisory Board, and Independent Opinion	Both Direct and Indirect
Quality of Learning Resources	Faculty, Students, and Advisory Board	Indirect
The Extent to which CLOs have been Achieved	Faculty, Program Leaders, Advisory Board, and Independent Opinion	Direct (as in section B) and Indirect/Surveys
	Students	Indirect
Other	-	-

Assessors (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify))

Assessment Methods (Direct, Indirect)





G. Specification Approval

COUNCIL /COMMITTEE	
REFERENCE NO.	
DATE	

