University of Tabuk
College of Computer and Information Technology
Department of Computer Science

Syllabus

Course Title: Computer Architecture

Course Code: CEN-312

Credit Hours: 3-0-0-3

Pre-Requisites: CSC-210

Text books:

Computer Organization and Architecture, William Stallings, Prentice Hall, ISBN: 0-13-081294-3

References:

The Architecture of Computer Hardware and Systems Software, Irv Englander, Third Edition, Willey, ISBN:0-471-07325-3
Systems Architecture, Stephen Burd, Course Technology, ISBN: 0-619-03418-1

Course Description:

This course provides deeper look on the structure and operation of computers. It is concerned with the operational methods of the hardware; the services provided by operating system software; the acquisition, processing, storage, and output of data; and the interaction between computers.

Learning Objectives:

Upon successful completion, students will be able to:

- Distinguish between Micro-programmed and Hardwired processor control, and describe the benefits of each approach;
- Describe the organization of RAM;
- Distinguish between Directly-Mapped Cache, Associative Cache, and Set-Associative Cache, and describe the principal issues related to cache memory organization;
- Describe the importance of the hit ratio to the effectiveness of the cache memory;
- Distinguish between virtual memory schemes based upon segmentation and based upon paging;
- Describe the differences between asynchronous and synchronous buses, as well as the importance of bus arbitration schemes to the effective operation of the bus;
- Analyze the nature of a computer instruction set, explore the interaction between the CPU -memory and I/O peripheral devices.

Method of Teaching

15 weeks (2 hrs per week) of lectures
15 weeks (2 hrs per week) of lab

Assessment / Evaluation:

Lab Work & Project	40%
Midterm Test	30%
Final Exam	30%
Total	100%

Course Outline

Week Topics/Contents

1 An Overview of Computer Systems
2 Bus Architectures
3 Cache Memory
4 Advanced RAM Organization
5 Secondary Storage
6 CPU structure and functions
7 Reduced Instruction Set Computer
8 Instruction level Parallelism and Superscaler Processor 9, 10 The IA-64 Architecture
11, 12 Control Unit Operation
13 Micro-programmed Control
14 Parallel Processing.
15 Review